REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on September 12, 2002, and the references cited therewith.

Claims 1, 4, and 5 are amended, and claims 32-53 are added; as a result, claims 1, 4-11, and 32-53 are now pending in this application.

§112 Rejection of the Claims

Claim 1 was rejected under 35 USC § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention.

Claim 1 is amended for clarity. Applicant believes that claim 1, as amended, particularly points out and distinctly claims the subject matter which Applicant regards as the invention. Accordingly, Applicant requests that the rejection be reconsidered and withdrawn.

§102 Rejection of the Claims

Claims 1 and 4-11 were rejected under 35 USC § 102(b) as being anticipated by Jeng et al. (U.S. Patent No. 5,710,073).

Claim 1 recites an "inner plug" and a pair of "outer plugs". In FIG. 2 of the present invention, the inner plug is element 206B and the pair of outer plugs are elements 206A and 206C. Jeng et al. discloses plugs 30A and plug 30B. On page 3 of the office action, plug 30B is being compared to inner plug 206B; plugs 30A are being compared outer plugs 206A and 206C. Claim 1 recites that the inner plug is isolated "beneath" and "between" the adjacent pair of the multiple surface structures. Jeng et al. shows plug 30B *not* being isolated "beneath" and "between" the adjacent pair of the multiple surface structures.

Claim 1 also recites that the outer plugs cover "part of top portions" of the adjacent pair. Plugs 30A of Jeng et al. *do not* cover "part of top portions" of the adjacent pair.

Claim 1 further recites a second conductive material, which "contacts" the inner plug and is isolated from the outer plugs by spacers. As indicated on page 4 of the office action, Jeng et al. shows a second conductive material 40 and spacers 38 (FIG. 8). However, second conductive

material 40 of *does not* contact plug 38B but is separated from plug 30B by layers 24, 26, and 28.

Based on the reasons presented above, Applicant believes that claim 1 is not anticipated by Jeng et at. Therefore, Application respectfully requests that the rejection of claim 1 be reconsidered and withdrawn and that claim 1 be allowed.

Claims 4-11 recite elements similar to the elements of claim 1. Thus, Applicant also believes that these claims are not anticipated by Jeng et at. Accordingly, Application requests that the rejections of claims 4-11 be reconsidered and withdrawn and that claims 4-11 be allowed.

New claims

New claims 32-53 were submitted in a Supplemental Preliminary Amendment filed on September 17, 2002 but were not considered. These new claims recite elements similar to the elements of claims 1 and 4-11. Thus, no new matter is introduced. Applicant resubmits these new claims in this amendment and response and requests consideration and allowance of these new claims. Applicant would also like to point out that these claims were also previously paid for in the Supplemental Preliminary Amendment.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's representative at (612) 373-6969 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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By their Representatives,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 11 day of December, 2002.

Tina Kohnert
Name

_____
Signature

Docket No. 303.645US3 Micron Ref. No. 98-0197.04
WD # 465138

CLEAN VERSION OF PENDING CLAIMS

METHOD AND STRUCTURE FOR IMPROVED ALIGNMENT TOLERANCE IN MULTIPLE, SINGULARIZED PLUGS
Applicant: Thomas A. Figura
Serial No.: 10/004,661

Claims 1, 4-11, and 32-53, as of December 11, 2002 (Date of Response to First Office Action).

Sub D1 C1

1. (Amended) An integrated circuit device on a substrate, comprising:

multiple semiconductor surface structures spaced apart along the substrate;

a number of plugs contacting the substrate between the multiple semiconductor surface structures, wherein the number of plugs includes an inner plug and a pair of outer plugs, wherein the inner and the pair of outer plugs are formed by the method of:

forming a first opening in a first isolation layer on the multiple semiconductor surface structures, wherein forming the first opening includes exposing portions of the multiple semiconductor surface structures, and includes exposing portions of the substrate between the multiple semiconductor surface structures;

depositing a first conductive material in the first opening to cover the multiple semiconductor surface structures;

forming a second isolation layer across the first conductive material;

etching the first conductive material and the second isolation layer to form a second opening in the first conductive material in a source region on the substrate, wherein the second opening exposes portions of an adjacent pair of the multiple semiconductor surface structures;

forming spacers on interior walls of the second opening, wherein forming the spacers includes separating the first conductive material into the inner plug and the pair of outer plug, wherein the inner plug is isolated beneath and between the adjacent pair, wherein the outer plugs cover part of top portions of the adjacent pair; and

forming a second conductive material in the second opening, whereby the second conductive material contacts the inner plug and is isolated from the outer plugs by the spacers.

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C2

2. ~~4.~~ (Amended) An integrated circuit comprising:

a first surface structure, a second surface structure, a third surface structure, and a fourth surface structure, each having a top surface;

an inner plug located in between the first and second surface structures and beneath the top surface of each of the first and second surface structures;

a first outer plug having an upper portion covered the top surface of each of the first and third surface structures, and a second outer plug having an upper portion covered the top surface of each of the second and four surface structures;

an inner electrical contact connected to the inner plug;

a first spacer for separating the inner plug and the inner electrical contact from the first outer plug, and a second spacer for separating the inner plug and the inner electrical contact from the second outer plug; and

an isolation for covering the inner electrical contact.

3. ~~5.~~ (Amended) The integrated circuit of claim 2 ~~4~~ further comprising a substrate connected to the first through fourth surface structures, the inner plug, and the first and second outer plugs.

6. The integrated circuit of claim 5, wherein the first through four surface structures are spaced apart along the substrate.

7. The integrated circuit of claim 4 further comprising a first outer contact region connected to the first outer plug.

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8. The integrated circuit of claim 7, wherein the first contact region is tapered.

9. The integrated circuit of claim 8 further comprising a second outer contact region connected to the second outer plug.

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10. The integrated circuit of claim 4, wherein the first and second outer plugs are on opposing sides of the inner plug.

NE

11. The integrated circuit of claim 10, wherein the first and second spacers are located on opposing sides of the inner plug.

32. (New) An integrated circuit comprising:

a plurality of surface structures, each of the surface structures having a top surface;

an inner plug formed between a pair of surface structures among the plurality of surface structures, and formed under the top surface of each surface structure of the pair of surface structures;

an inner electrical contact formed on the inner plug;

a pair of outer plugs, each outer plug of the pair of outer plugs having an upper portion formed over at least a portion of the top surface of one surface structure of the pair of surface structures; and

a pair of spacers formed between the pair of outer plugs and the inner plug and the inner electrical contact.

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33. (New) The integrated circuit of claim 32, further comprising an isolation layer formed around the inner electrical contact, the isolation layer being formed from insulating material.

34. (New) The integrated circuit of claim 32, wherein the inner plug is formed from conductive material.

35. (New) The integrated circuit of claim 34, wherein the pair of outer plugs are formed from conductive material.

36. (New) The integrated circuit of claim 32, wherein the pair of spacers are formed from insulating material.

37. (New) The integrated circuit of claim 32, wherein:

a first outer plug of the pair of outer plugs is formed on one side the inner plug; and

a second outer plug of the pair of outer plugs is formed on another side the inner plug.

38. (New) The integrated circuit of claim 32, wherein:

a first spacer of the pair of spacers is formed on one side the inner plug; and

a second spacer of the pair of spacers is formed on another side the inner plug.

39. (New) The integrated circuit of claim 32, wherein the surface structures are formed from semiconductor material.

40. (New) An integrated circuit comprising:

a plurality of surface structures formed over a substrate, each of the surface structures having a top surface;

an inner plug formed between a pair of surface structures among the plurality of surface structures and formed under the top surface of each surface structure of the pair of surface structures;

an inner electrical contact formed on the inner plug;

a first outer plug and a second outer plug, each of the first and second outer plugs having an upper portion formed over at least a portion of the top surface of one surface structure of the pair of surface structures; and

a pair of spacers, each spacer of the pair of pacers having a spacer portion formed over at least a portion of the top surface of one surface structure of the pair of surface structures for isolating the inner plug and the inner electrical contact from the first and second outer plugs.

41. (New) The integrated circuit of claim 40, further comprising an isolation structure formed around the inner electrical contact, the isolation structure being formed from insulating material.

42. (New) The integrated circuit of claim 41, further comprising an isolation layer formed over the first and second outer plugs.

43. (New) The integrated circuit of claim 40, wherein the inner plug is formed from conductive material.

44. (New) The integrated circuit of claim 43, wherein the pair of spacers are formed from insulating material.

45. (New) The integrated circuit of claim 40 further comprising:

a first contact region formed through the isolation layer and connected to the first outer plug; and

a second contact region formed through the isolation layer and connected to the second outer plug.

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46. (New) The integrated circuit of claim 45, wherein the first and second outer plugs are formed from conductive material.

47. (New) The integrated circuit of claim 46, wherein the first and second contact regions are formed from conductive material.

48. (New) The integrated circuit of claim 47, wherein each of the first and second contact regions is tapered.

49. (New) An integrated circuit comprising:

a plurality of surface structures formed over a substrate each of the of surface structures having a top surface;

an inner plug of conductive material formed between a pair of surface structures among the plurality of surface structures and formed under the top surface of each surface structure of the pair of surface structures;

an inner electrical contact formed on the inner plug for proving electrical connection to the inner plug, wherein the inner electrical contact is buried in an isolation layer;

a first outer plug of conductive material and a second outer plug of conductive material, each of the first and second outer plugs having an upper portion covering at least a portion of the top surface of one surface structure of the pair of surface structures; and

a pair of spacers of insulating material formed between the inner plug and the inner electrical contact and the first and second outer plugs.

50. (New) The integrated circuit of claim 49, wherein the inner electrical contact forms a conductive line for electrically connecting to the storage node plugs via the substrate.

51. (New) The integrated circuit of claim 49, wherein the surface structures includes a plurality of conductive lines for creating electrical contacts between the inner electrical contact and the first and second storage node plugs and via the substrate.

52. (New) The integrated circuit of claim 49 further comprising a second isolation layer formed over the first and second outer plugs.

53. (New) The integrated circuit of claim 52 further comprising:

a first contact region formed through the isolation layer and connected to the first outer

plug; and

a second contact region formed through the isolation layer and connected to the second outer plug.